30. (Amended) The semiconductor device according to claim 29, wherein said at least one island of single crystal silicon comprises a plurality of islands and said at least one isolation oxide comprises a plurality of isolation oxides, and each of said islands are interspaced between said isolation oxides to form a shallow trench isolation (STI) structure.

Sub I2

31. (Amended) The semiconductor device according to claim 30, wherein said insulator layer has a thickness in a range of 1000Å and 5000Å.

A2

32. (Amended) The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon is formed over said insulator layer by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon, and crystallizing said amorphous silicon by using said lower portion of said single crystal silicon as a crystal growth seed.

33. (Amended) The semiconductor device according to claim 32, wherein said isolation oxides are formed in defective portions of said single crystal silicon.

34. (Amended) The semiconductor device according to claim 31, wherein said isolation oxides and said insulator layer are formed of a same material.

35. (Amended) The semiconductor device according to claim 29, wherein an upper surface of said isolation oxides and said single crystal silicon are planarized.

36. (Twice Amended) The semiconductor device according to claim 29, wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

37. The semiconductor device according to claim 29, further comprising:

a memory device formed in said bulk silicon region; and

a logic device formed in said SOI region.

38. The semiconductor device according to claim 37, wherein said memory device comprises at least one of a dynamic random access memory (DRAM) device, a memory array, a static random access memory (SRAM) device, a flash memory device, a high voltage, high power circuit, and an analog circuit.

39. The semiconductor device according to claim 37, wherein said logic device comprises at least one of a logic circuit, a P-FET device, an N-FET device, a low voltage, low power circuit, and a high performance digital circuit.

Sub H2 F3

41. (Four Times Amended) A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

an insulator layer which is formed beneath an upper portion of single crystal silicon and has at least one lateral end portion adjacent a lower portion of said single crystal silicon; and

a plurality of isolation oxides formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein said upper portion of said single crystal silicon and said lower portion of said single crystal silicon have a same crystal orientation.

Sub H5 F4

42. (Amended) The hybrid substrate according to claim 41, wherein said insulator layer is formed only in an SOI region of said substrate and not in a bulk silicon region of said substrate.

43. (Amended) The hybrid substrate according to claim 42, wherein said substrate is part of a semiconductor device comprising a logic device formed in said silicon-on-insulator (SOI) region.

44. (Amended) The hybrid substrate according to claim 42, wherein said substrate is part of a semiconductor device comprising a memory device formed in said bulk silicon region.

45. (Four Times Amended) A semiconductor device comprising:

a bulk semiconductor region comprising semiconductor substrate; and

a semiconductor-on-insulator region comprising:

an insulator layer which is formed beneath an upper portion of said semiconductor substrate and has at least one lateral end portion adjacent to a lower portion of said semiconductor substrate; and

at least one isolation oxide formed in said upper portion of said semiconductor substrate so as to form at least one island of said semiconductor substrate on an upper surface of said insulator layer,

wherein said upper portion of said semiconductor substrate and said lower portion of said semiconductor substrate have a same crystal orientation.

46. (Thrice Amended) A semiconductor device comprising:

a single crystal silicon substrate having a lower portion and an upper portion;

an insulator layer which is formed beneath said upper portion of said single crystal silicon substrate and has at least one lateral end portion adjacent to said lower portion of said single crystal silicon substrate; and

at least one isolation oxide formed in said upper portion of said single crystal silicon substrate so as to form at least one island of said single crystal silicon substrate on an upper surface of said insulator layer,

wherein said upper portion of said single crystal silicon substrate and said lower portion of said single crystal silicon substrate have a same crystal orientation.

47. The semiconductor device according to claim 46, wherein said upper portion of said single crystal silicon substrate is formed on said insulator layer by growing said single crystal silicon substrate horizontally over said insulator layer.

48. The semiconductor device according to claim 46, wherein said upper portion of said single crystal silicon is formed by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon substrate, annealing said amorphous silicon so that, using said lower portion of said single crystal silicon substrate as a crystal growth seed, said amorphous silicon is converted to single crystal silicon having a same orientation as said lower portion of said single crystal silicon substrate.

49. The semiconductor device according to claim 48, wherein said isolation oxides are formed by forming isolation trenches in defective portions of said upper portion of said single crystal silicon, and depositing oxide in said isolation trenches.

Please add the following new claims:

- - 50. The semiconductor device according to claim 29, wherein an angle between a bottom surface of said insulator layer and a sidewall of said insulator layer is about 103°.

51. The semiconductor device according to claim 29, wherein a crystal orientation and structure of said upper portion of said single crystal silicon follows a crystal orientation and structure of said lower portion of said single crystal silicon.

52. The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon comprises crystallized amorphous silicon.

53. The semiconductor device according to claim 29, wherein said insulator layer has a width in a range of about 2 μm to 10 μm.

54. The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon has a thickness in a range of about 500 Å to 3000 Å. - -